Amendments to the Claims

A complete list of pending claims follows, with indicated amendments:

1. (Previously Amended) A method for handling system management interrupts in a multiprocessor computer system, wherein each processor of the multiple processors of the computer system is operable to process a system management interrupt, comprising the steps of:

writing a predetermined signature to a predetermined register of a first processor;

executing in the first processor a command of a software application to cause the first processor to initiate a system management interrupt;

receiving at each processor an instruction that the system management interrupt has been issued;

entering system management mode at each processor;

saving register contents of each processor to a memory space associated with each respective processor;

selecting from among the multiple processors a second processor as a system management interrupt handler, the selection of the second processor being accomplished according to an arbitration scheme;

scanning the contents of the memory space associated with each processor; and

when the selected second processor locates the saved predetermined signature in one of the memory spaces associated with the processors of the computers system, using the contents of the memory space associated with the predetermined signature for any parameters necessary for the handling of the system management interrupt.

2-3. (Cancelled).

4. (Currently Amended) The method for issuing and handling system management interrupts in the multiprocessor computer system of claim 1, wherein the first processor and the second processor are ~~a~~ the same processor.

5. (Previously Amended) The method for issuing and handling system management interrupts in the multiprocessor computer system of claim 1, wherein the step of executing in the first processor the command of the software application to cause the first processor to initiate the system management interrupt comprises the step of executing a software instruction causing the first processor to write to a predetermined port of a chip set of the computer system.

6. (Previously Amended) The method for issuing and handling system management interrupts in the multiprocessor computer system of claim 5, wherein the predetermined port of the chip set resides in a PCI bridge of the chip set.

7. (Previously Amended) The method for issuing and handling system management interrupts in the multiprocessor computer system of claim 5, wherein the predetermined port of the chip set resides in an expansion bridge of the chip set.

8. (Previously Amended) The method for issuing and handling system management interrupts in the multiprocessor computer system of claim 7, further comprising the step of

issuing from the expansion bridge the instruction causing each of the processors of the system to enter system management mode.

9-15. (Cancelled).

16. (Currently Amended) A method for handling system management interrupts in a multiprocessor computer system in which each of the processors of the computer system is operable to handle software system management interrupts, comprising the steps of:

issuing an instruction from a first processor of the system to a chip set of the computer system;

receiving the instruction at the chip set of the computer system and, in response, issuing a command causing the processors of the system to enter system management mode;

writing a software system management interrupt signature to a predetermined register of the first processor as an indication that the first processor issued the command that caused the processors of the system to enter system management mode;

writing contents of the registers of each processor to a memory location, the memory location including a memory space reserved for and associated with the register contents of each processor;

selecting a second processor, the selection of the second processor as the system management interrupt handler being accomplished according to an arbitration scheme;

transmitting a software system management interrupt to the second processor of the computer system, the second processor including a system management interrupt handler, and

the second processor locating, in response~~,~~ to the receipt of the software system management interrupt, the software system management interrupt signature in the memory location; and

retrieving for use by the system management interrupt handler as parameters register contents saved by the first processor to the memory space associated with the software system management interrupt.

17-18. (Cancelled).

19. (Previously Amended) The method for handling system management interrupts in the multiprocessor computer system of claim 16, wherein the instruction from the first processor to the chip set of the computer system is a write command to a predetermined port of the chip set.

20. (Previously Amended) The method for handling system management interrupts in the multiprocessor computer system of claim 19, wherein the write command is received and the software system management interrupt is issued by a PCI bridge of the chip set.

21. (Previously Amended) The method for handling system management interrupts in the multiprocessor computer system of claim 19, wherein the write command is received and the software system management interrupt is issued by an expansion bus bridge of the chip set.

22. (Currently Amended) A method for handling a system management interrupt in a multiprocessor computer system, wherein each of the multiple processors of the computer system ~~are~~ is capable of operating as a system management interrupt handler, comprising the steps of:

receiving at each of the processors an instruction to enter a mode associated with the issuance of a system management interrupt;

selecting a designated processor from among the set of processors capable of operating as a system management interrupt handler, as a system management interrupt handler, the selection of the designated processor being accomplished according to an arbitration scheme;

scanning the memory location containing saved contents of each processor of the computer system;

locating in the memory location a signature identifying the saved contents of the processor that issued an instruction that caused the system management interrupt; and

retrieving from the saved contents of the issuing processor parameters necessary for handling of the system management interrupt.

23. (Previously Amended) The method for a handling system management interrupt in the multiprocessor system of claim 22, wherein the designated processor is not the processor that issued the instruction that caused the system management interrupt.

24-27. (Cancelled).